



US006145036A

United States Patent [19][11] **Patent Number:** 6,145,036**Barenys et al.**[45] **Date of Patent:** Nov. 7, 2000[54] **POLLING OF FAILED DEVICES ON AN I²C BUS**[75] **Inventors:** Michael Anton Barenys, Austin;
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Gerard Goodwin; Forrest Clifton
Gray, both of Austin, all of Tex.[73] **Assignee:** International Business Machines
Corp., Armonk, N.Y.[21] **Appl. No.:** 09/163,918[22] **Filed:** Sep. 30, 1998[51] **Int. Cl.⁷** G06F 13/00; G06F 11/00[52] **U.S. Cl.** 710/101; 710/2; 710/126;
710/129; 714/25; 714/48[58] **Field of Search** 710/2, 3-19, 36-45,
710/101-103, 104-112, 126-131; 714/2,
8, 25, 48-57; 711/200[56] **References Cited****U.S. PATENT DOCUMENTS**

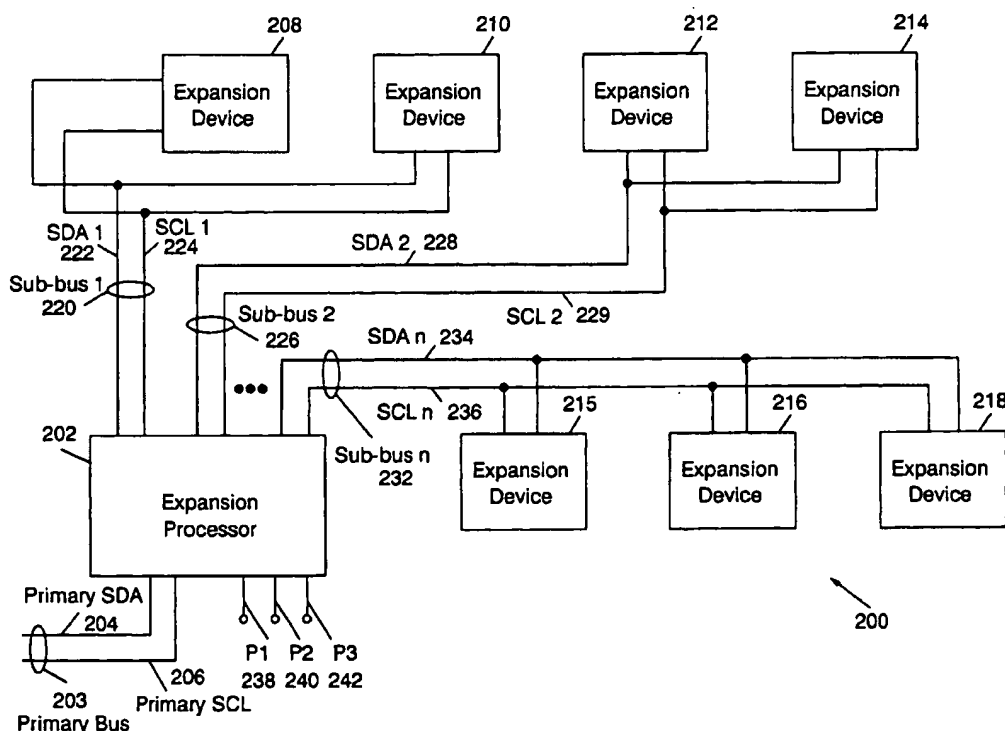
5,613,157	3/1997	Davidson et al.	710/8
5,764,968	6/1998	Ninomiya	713/601
5,892,933	4/1999	Voltz	710/131
5,897,663	4/1999	Stancil	711/200
5,907,557	5/1999	Gandar	370/475
5,913,045	6/1999	Gillespie et al.	710/129
5,987,554	11/1999	Liu et al.	710/129

FOREIGN PATENT DOCUMENTS

WO 98/34376 8/1998 WIPO H04L 12/20

Primary Examiner—Christopher B. Shin**Attorney, Agent, or Firm**—Kelly K. Kordzik; Winstead
Sechrest & Minick; Leslie A. Van Leeuwen[57] **ABSTRACT**

Polling of devices on an inter-IC (I²C) is provided. An expansion processor resides on a primary I²C bus. The expansion processor is coupled to a plurality of I²C sub-buses each of which may host a plurality of I²C devices. Data is transferred between the expansion processor and the plurality of I²C devices via the corresponding sub-bus according to an I²C protocol. Data transfer is in response to a request initiated by a bus master on the primary I²C bus. The bus master communicates with a target device residing on one of the sub-buses by addressing the expansion processor. The bus master informs the expansion processor of the target device by sending the expansion processor a number of the sub-bus on which the target device resides, and an address of the target device. A data stream bound for the target device is directed to the expansion processor which then echos it to the target device. Likewise, a data stream bound from the target device to the bus master on the primary I²C bus is transmitted to the expansion processor which then echos it to the bus master. Each of the target devices on the sub-bus can be polled to determine if they have failed. Failure of a device only affects operation of its sub-bus.

15 Claims, 7 Drawing Sheets

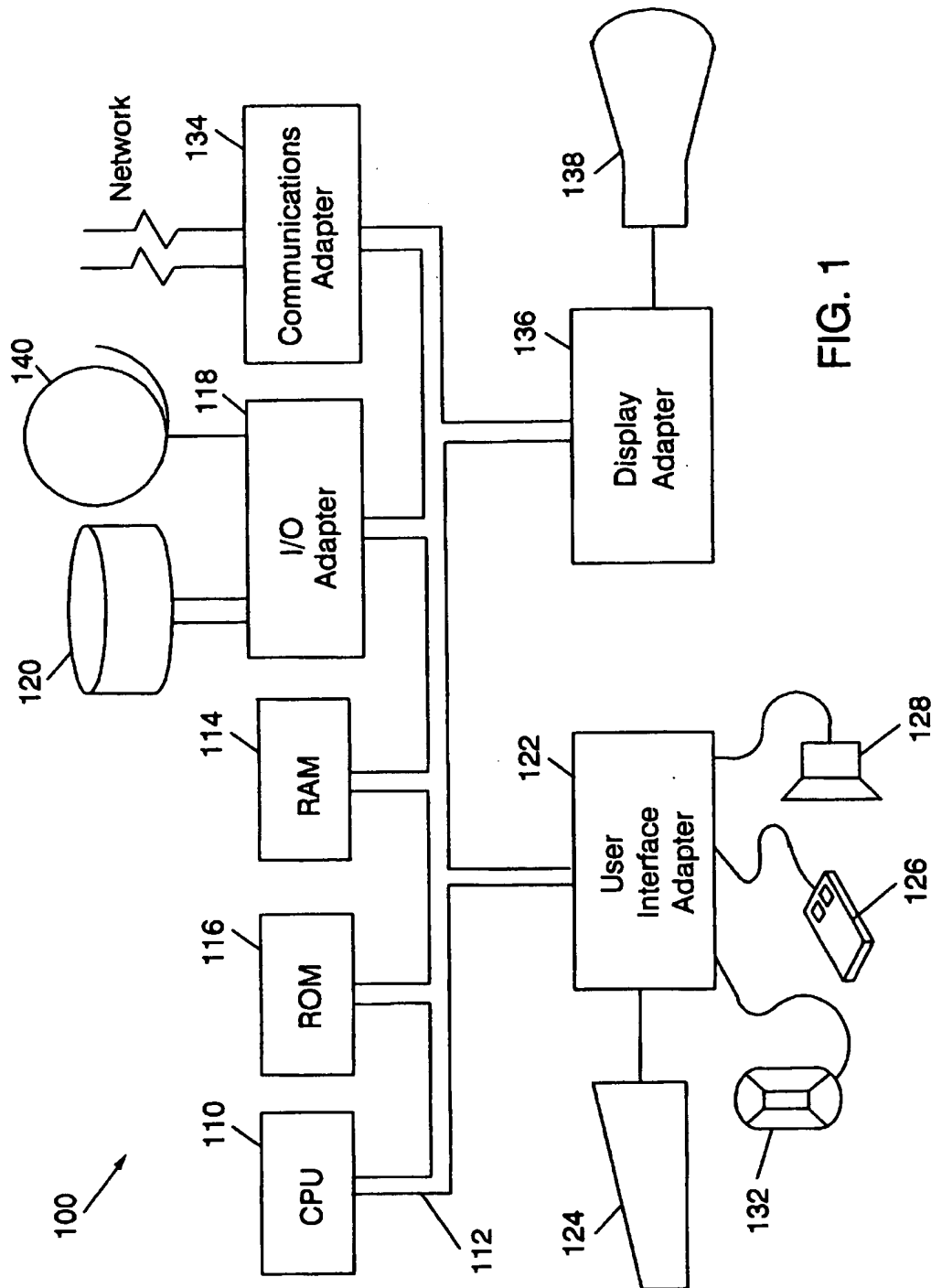


FIG. 1

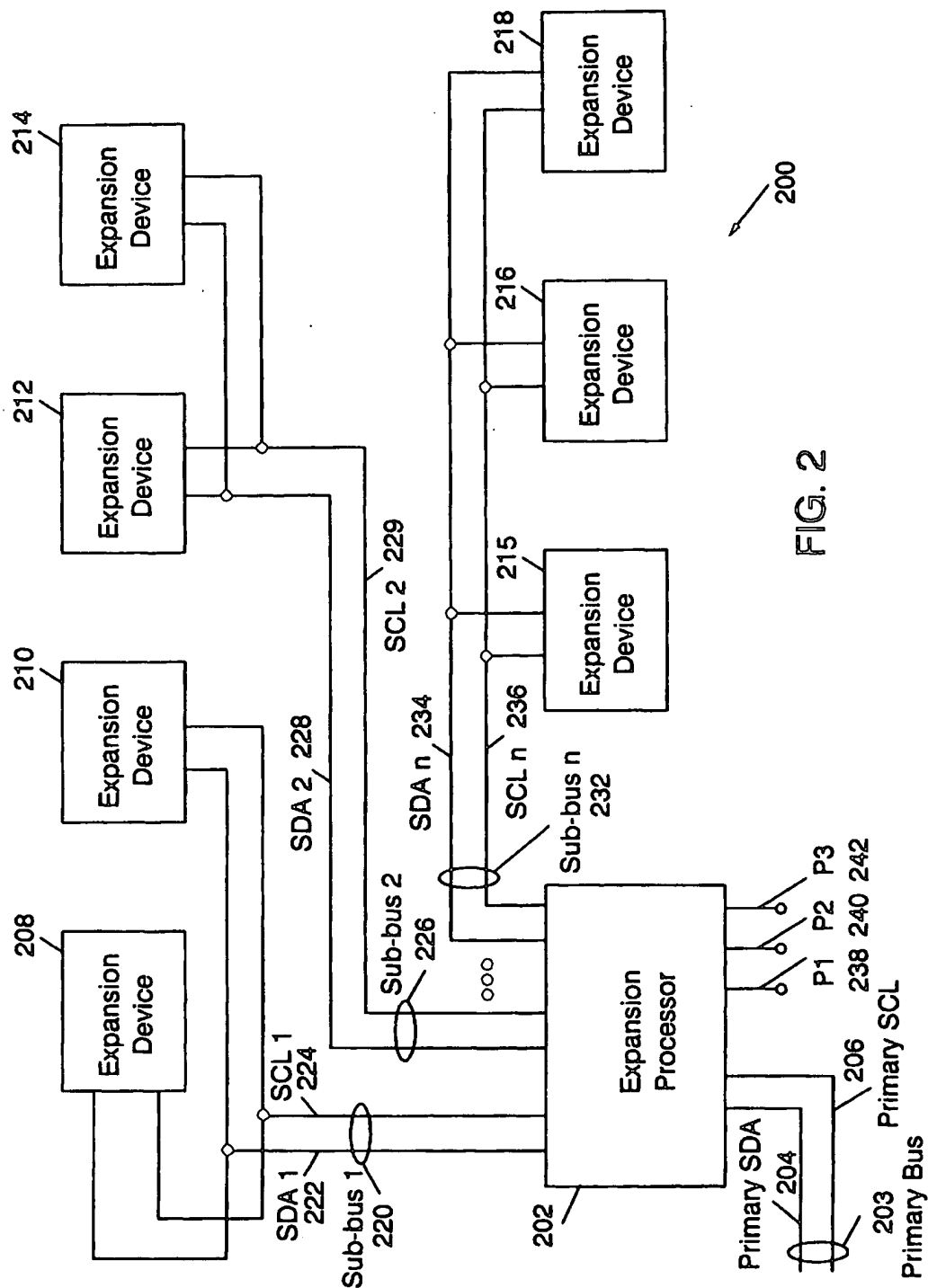


FIG. 2

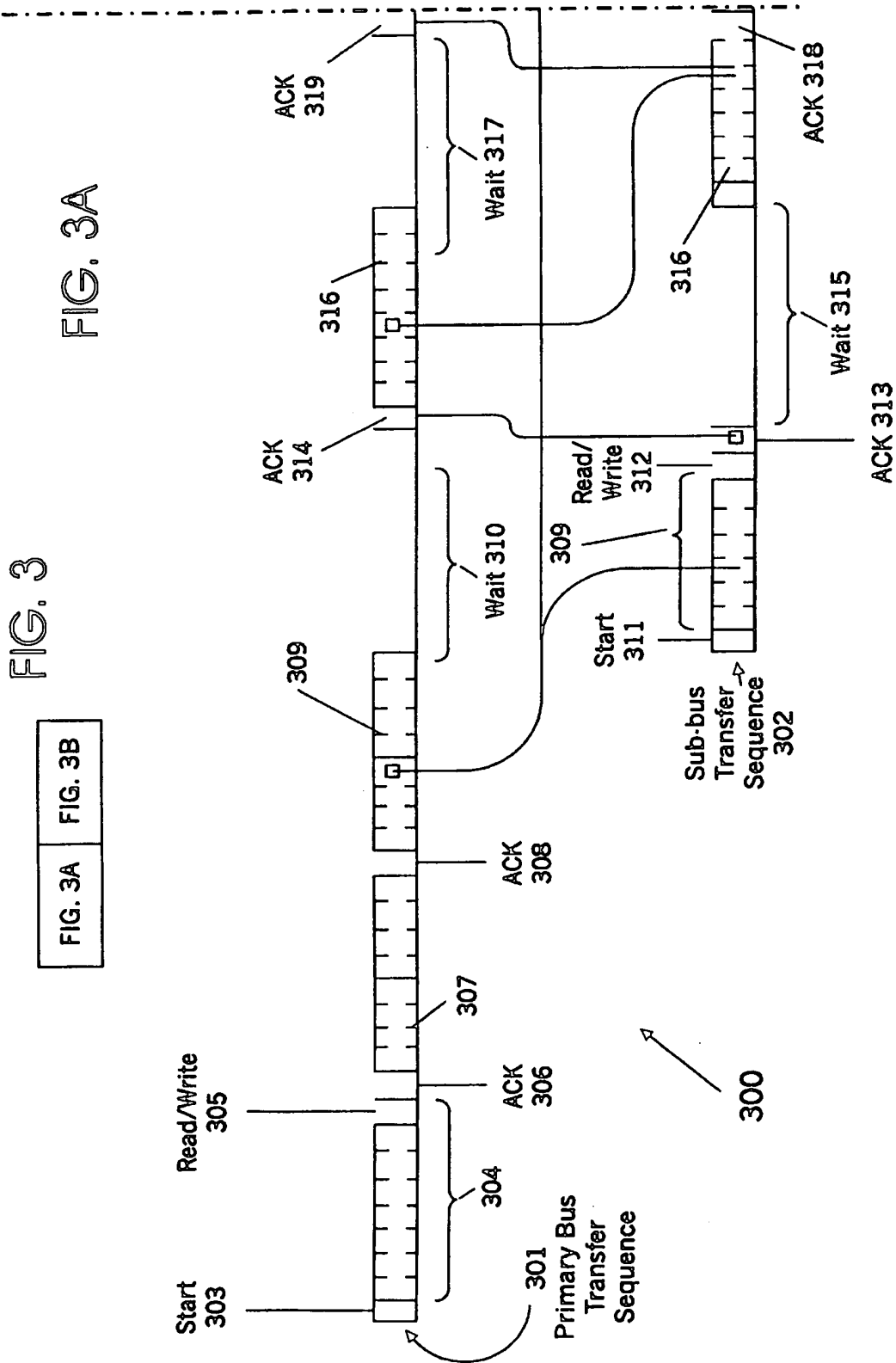


FIG. 3B

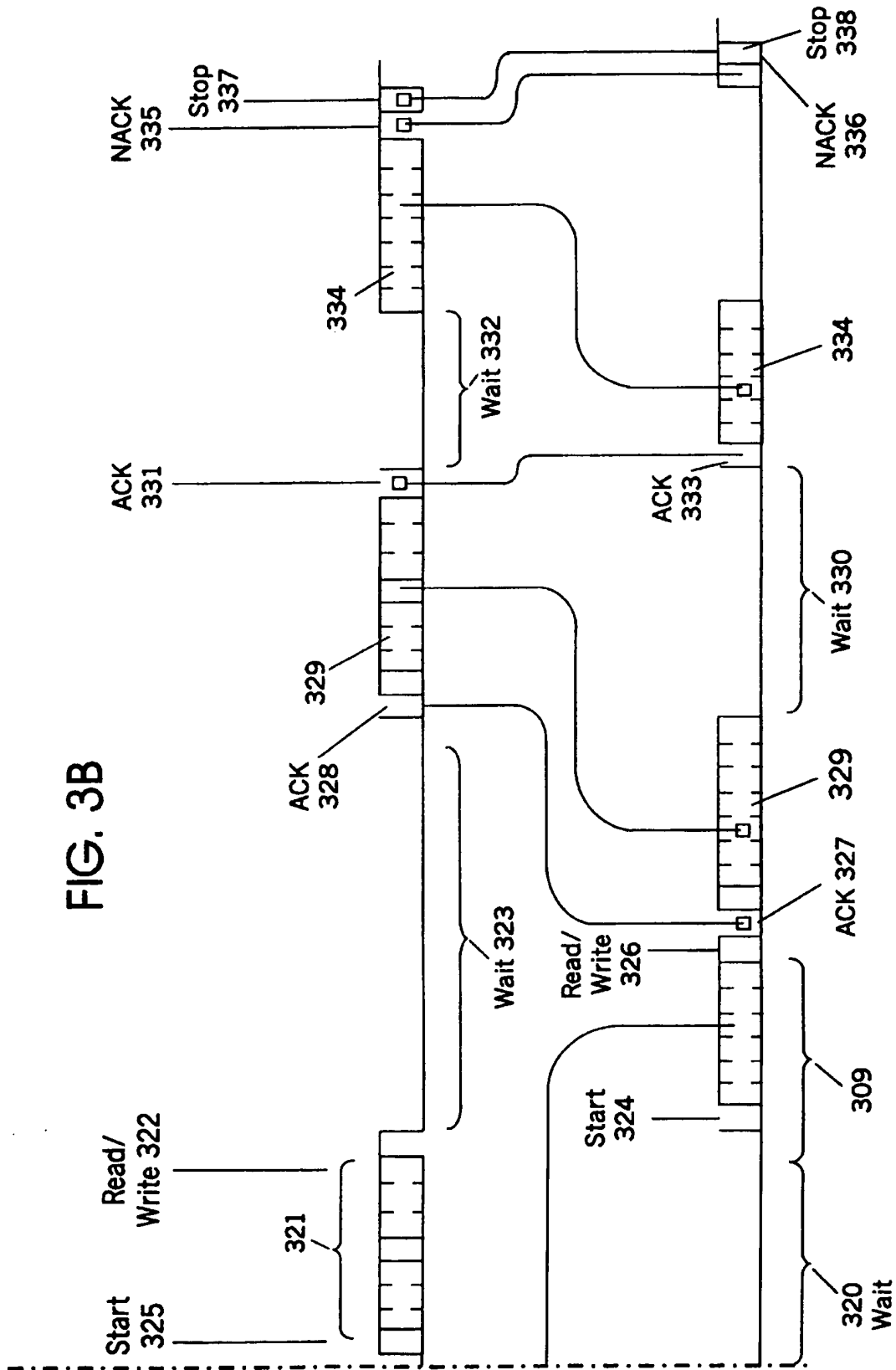
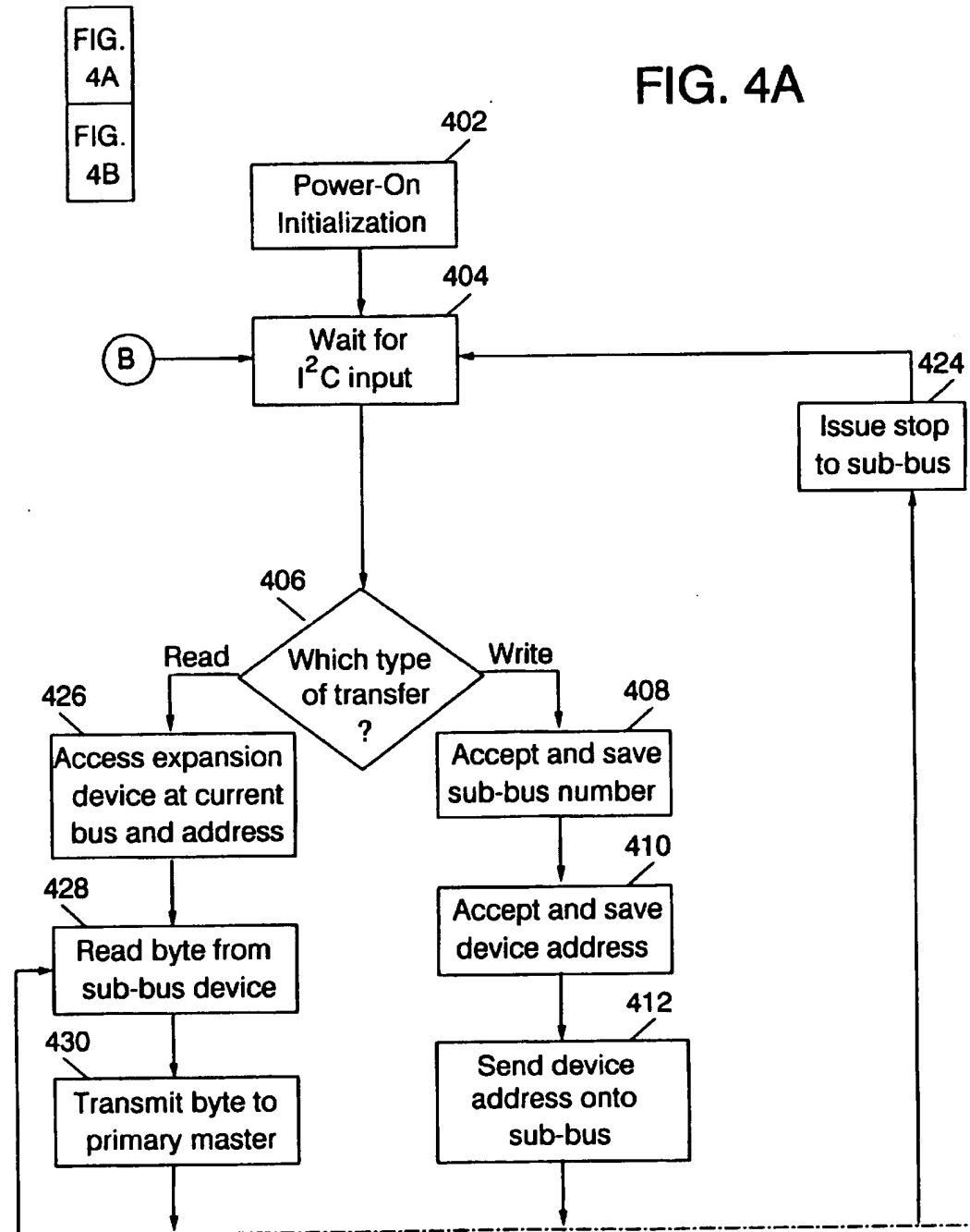


FIG. 4



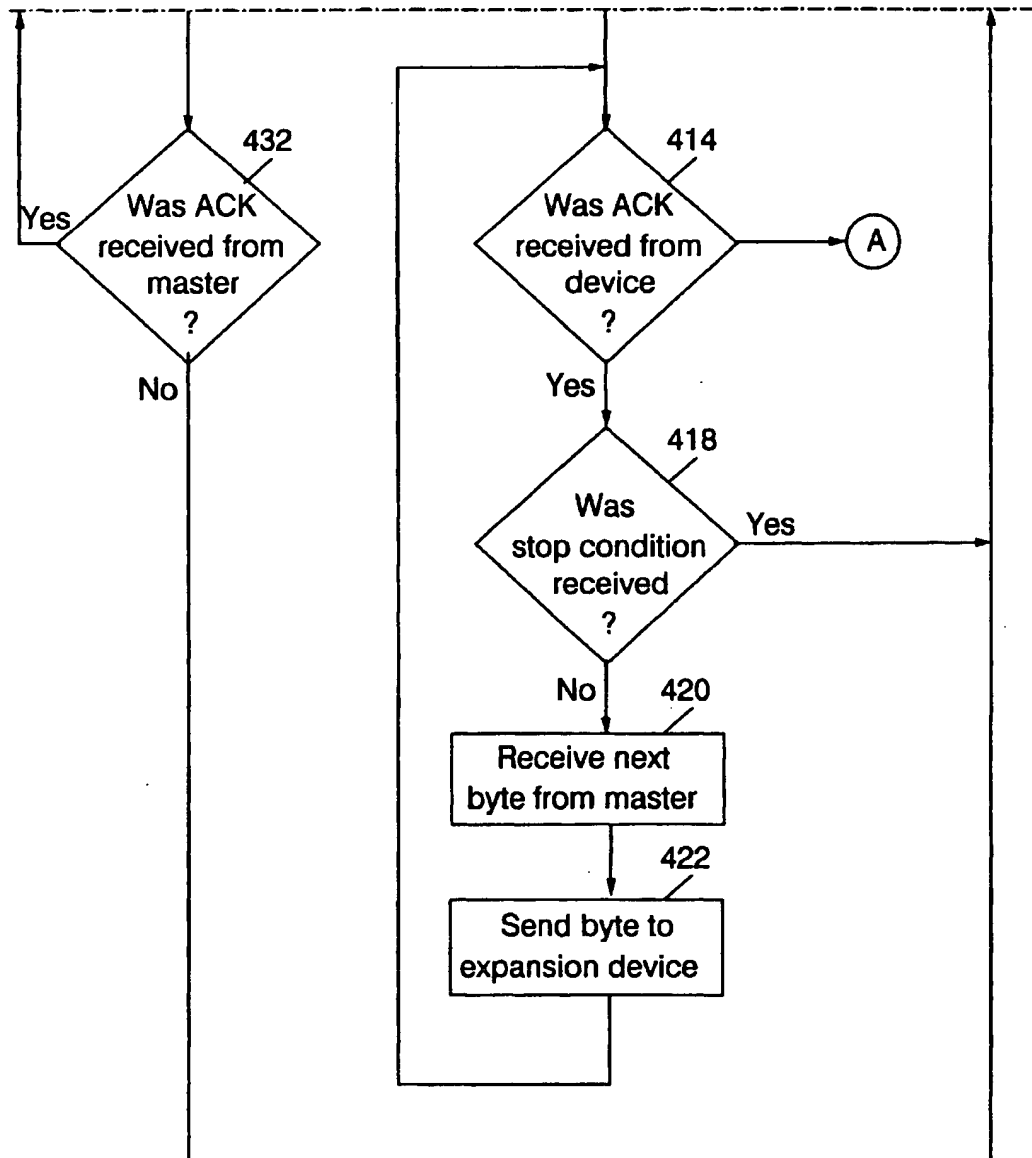
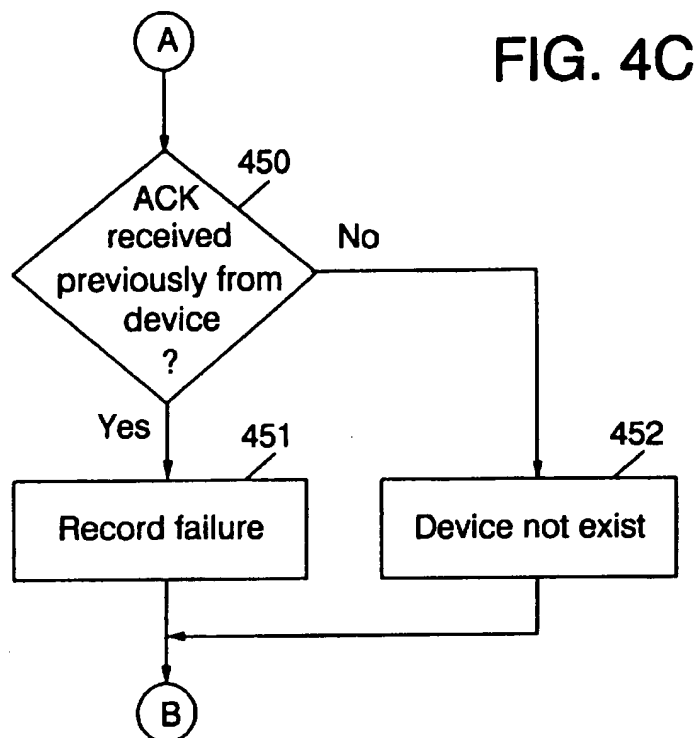
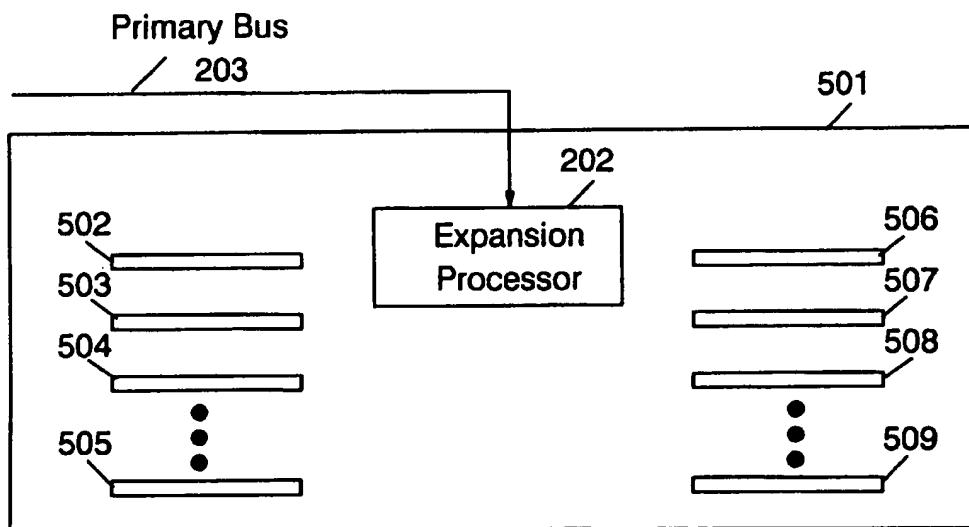


FIG. 4B

400

**FIG. 5**

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POLLING OF FAILED DEVICES ON AN I²C BUS

CROSS REFERENCE TO RELATED APPLICATIONS

The present invention is related to U.S. patent application Ser. No. 09/163,992, entitled "AN I²C BUS EXPANSION APPARATUS AND METHOD THEREFOR," and U.S. patent application Ser. No. 09/164,126, entitled "EXTERNALLY PROVIDED CONTROL OF AN I²C BUS," which are hereby incorporated by reference herein.

TECHNICAL FIELD

The present invention relates in general to data processing systems, and in particular, to an inter-IC (I²C) bus in a data processing system.

BACKGROUND INFORMATION

The I²C bus is a 2-wire bidirectional serial bus for communication between bus devices in a data processing system. Bus devices may include microprocessors, microcontrollers, memory devices, peripheral devices, data converters, and application oriented circuits. Two wires of the I²C bus constitute a serial data line (SDA) for communicating data between bus devices, and a serial clock line (SCL) carrying clock signals that control bus access and data transfer.

Each device on the I²C bus is identified by a unique address. The least significant bit (LSB) of an address byte constitutes a read/write (R/W) bit that signals whether the current bus transaction is a read operation or a write operation. Of the remaining seven bits, four denote the functional group to which the bus device belongs, leaving three bits which may be freely assigned to form the unique address of the particular bus device. Thus, within a particular device group, or category, eight devices from within the group may reside on a given I²C bus.

Many systems use the I²C bus to determine the hardware make-up of a system. The various removable components that constitute the system are connected together on the I²C bus. Each component contains an I²C device that provides information about itself to the system. For example, each device may have a EEPROM module containing vital product data ("VPD") information stored thereon. All of the components in the system are connected on the single I²C bus. The system gathers information about the components by polling the various devices on the I²C bus. The drawback is that in cases where there is a failure on one of the devices in the system, the failure can potentially cause the entire I²C bus to fail (the I²C bus will be locked up when the device fails by pulling the SDA and SCL lines of the I²C bus to ground). This makes it impossible to isolate the failing device in the system.

Customers increasingly demand that computers be easily serviced, in order to reduce the amount of down-time on the system. It is therefore critical to find a method that allows for better failure isolation in such cases.

SUMMARY OF THE INVENTION

The foregoing needs are addressed by the present invention, which uses an I²C bus expander to isolate the various buses in the system and thereby contain the bus failure to one component in the system. The bus expander takes a primary I²C bus and feeds the data to a series of secondary buses (sub-buses). Each replaceable component

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in the system can contain several I²C sub-buses and is connected to its own primary I²C bus. In this manner, a failing device on one of the components will not cause a failure on the entire primary I²C system bus. This also allows the system to identify the failing component for replacement. This type of isolation allows for better fault detection in the system while increasing the number of devices which can be connected to one bus.

The foregoing has outlined rather broadly the features and technical advantages of the present invention in order that the detailed description of the invention that follows may be better understood. Additional features and advantages of the invention will be described hereinafter which form the subject of the claims of the invention.

BRIEF DESCRIPTION OF THE DRAWINGS

For a more complete understanding of the present invention, and the advantages thereof, reference is now made to the following descriptions taken in conjunction with the accompanying drawings, in which:

FIG. 1 illustrates, in block diagram form, a data processing system in accordance with one embodiment of the present invention;

FIG. 2 illustrates, in block diagram form, an I²C bus expansion apparatus in accordance with one embodiment of the present invention;

FIGS. 3A-3B schematically illustrate an I²C bus expansion transfer sequence in accordance with an embodiment of the present invention;

FIGS. 4A, 4B and 4C illustrate, in flowchart form, an I²C bus expansion method in accordance with one embodiment of the present invention; and

FIG. 5 illustrates a memory device configured in accordance with the present invention.

DETAILED DESCRIPTION

In the following description, numerous specific details are set forth such as clock intervals and data sequence lengths, etc. to provide a thorough understanding of the present invention. However, it will be obvious to those skilled in the art that the present invention may be practiced without such specific details. In other instances, well-known circuits have been shown in block diagram form in order not to obscure the present invention in unnecessary detail. For the most part, details concerning timing considerations and the like have been omitted inasmuch as such details are not necessary to obtain a complete understanding of the present invention and are within the skills of persons of ordinary skill in the relevant art.

Refer now to the drawings wherein depicted elements are not necessarily shown to scale and wherein like or similar elements are designated by the same reference numeral through the several views.

A representative hardware environment for practicing the present invention is depicted in FIG. 1, which illustrates a typical hardware configuration of data processing system 100 in accordance with the subject invention having central processing unit (CPU) 110, such as a conventional microprocessor, and a number of other units interconnected via system bus 112. A portion of system bus 112 may be a primary I²C bus, to be discussed in conjunction with FIG. 2. Data processing system 100 includes random access memory (RAM) 114, read only memory (ROM) 116, and input/output (I/O) adapter 118 for connecting peripheral devices such as disk units 120 and tape drives 140 to bus

112, user interface adapter 122 for connecting keyboard 124, mouse 126, and/or other user interface devices such as a touch screen device (not shown) to bus 112, communication adapter 134 for connecting data processing system 100 to a data processing network, and display adapter 136 for connecting bus 112 to display device 138. CPU 110 may include other circuitry not shown herein, which will include circuitry commonly found within a microprocessor, e.g., execution unit, bus interface unit, arithmetic logic unit, etc. CPU 110 may also reside on a single integrated circuit.

Refer now to FIG. 2 in which is illustrated I²C expansion apparatus 200 in accordance with the principles of the present invention. Expansion processor 202 resides on primary I²C bus 203 which includes primary SDA 204 and primary SCL 206. An embodiment of expansion processor 202 may include a conventional microcontroller having I²C compatibility such as an 83C751 or, alternatively, 87C751, microcontroller manufactured by Philips Semiconductors. (These two devices differ only in the form of internal program memory.) Expansion processor 202 may be an I²C slave responding to requests from a I²C bus master residing on primary I²C bus 203. A bus master on primary bus 203 may initiate requests for an I²C transaction (either a read or a write) to a plurality of expansion devices 208, 210, 212, 214, 216, and 218. These expansion devices may include any I²C compatible device, and may include, but are not necessarily limited to, microprocessors, gate arrays, liquid crystal display (LCD) drivers, memory, data converters, network drivers/adapters, and application oriented devices.

Alternatively, any one or more of expansion devices 208, 210, 212, 214, 216, and 218 may be another expansion processor, such as expansion processor 202, coupled by one or more sub-buses to one or more expansion devices.

Moreover, the I²C expansion apparatus 200 illustrated in FIG. 2 may be implemented on one or more of a plurality of devices coupled to a data processing system, such as, but not limited to, microprocessors, gate arrays, liquid crystal display drivers, memory modules, data converters, network adapters, and application oriented devices.

For example, referring to FIG. 5, there is illustrated memory chip 501 having an expansion processor 202 connected to primary bus 203. Memory chip 501 contains a plurality of memory modules 502-509, which may be dual in-line memory modules (DIMMs). Though not shown in FIG. 5 for reasons of clarity, each of the DIMMs 502-509 will include a EEPROM containing vital product data (VPD) information, which may include particular information about the DIMM. Each of these EEPROMs will be connected by an I²C sub-bus to the expansion processor 202.

In previous implementations, a failure on any one of the memory DIMMs could potentially cause a failure on the main I²C bus in the system, making it impossible to determine the failing part. And, as a result, to find the failing DIMM would require a manual replacement of all of the components in the system until the failing DIMM was found. With the present invention, it is possible to determine which sub-bus is causing a failure to more effectively isolate the problem. With the present invention, if a DIMM fails, then only its particular sub-bus will fail, resulting in the other sub-buses not failing and correspondingly, no failure in the primary bus 203.

Please note that FIG. 2 illustrates a plurality of expansion devices on one particular sub-bus (e.g., expansion devices 215, 216, and 218 on sub-bus 232). However, the present invention may be implemented where every expansion device is on a separate sub-bus. For example, each of the

DIMMs 502-509 may be connected to expansion processor 202 by a separate I²C sub-bus to facilitate isolation of errors in accordance with the present invention.

Communications between a bus master on primary bus 203 and one of the expansion devices is mediated by expansion processor 202. Each of expansion devices 208, 210, 212, 214, 216 and 218 is coupled to expansion processor 202 by one of a plurality of I²C sub-buses, sub-bus 220 through sub-bus 230. Each sub-bus includes a two-wire pair. Sub-bus 220 includes SDA 222 and SCL 224, coupling expansion devices 208 and 210 to expansion processor 202. Similarly, sub-bus 226 includes SDA 228 and SCL 229 which couples expansion devices 212 and 214 to expansion processor 202. Sub-bus 232 includes SDA 234 and SCL 236 coupling expansion processor 202 to expansion devices 215, 216 and 218. In an embodiment of the present invention in which expansion processor 202 is implemented with a conventional microcontroller, sub-buses 220, 226 and 232 may be driven from device input/output (I/O) pins. It would be understood by one of ordinary skill in the art that each of sub-buses 220, 226 and 232 may couple other numbers of expansion devices to expansion processor 202 consistent with I²C addressing specifications.

In operation, a bus master on primary bus 203 communicates with one of the expansion devices by addressing expansion processor 202. Expansion processor 202 is assigned a preselected I²C address as an I²C device on primary bus 203. In an embodiment of the present invention, the I²C address of expansion processor 202 on primary bus 203 may be assigned by programming a plurality of pins, P1 238, P2 240, and P3 242. In one embodiment of the present invention, pins 238, 240, and 242 may be dynamically programmed with a preselected address by, for example, CPU 110 in data processing system 100 of FIG. 1. Alternatively, pins 238, 240 and 242 may be statically programmed by coupling them to an appropriate voltage supply. In another embodiment of the present invention in which expansion processor 202 is a conventional microcontroller, pins 238, 240 and 242 may be a preselected set of input/output (I/O) pins wherein pins 238, 240 and 242 may be programmed with a binary address by coupling the pins to voltage supplies representing a logic "1" and a logic "0", respectively. Such static programming, would be understood by one of ordinary skill in the art.

Pins 238, 240 and 242 may be sampled by expansion processor 202 following reset and the resulting address stored internally. Note that in an embodiment of expansion processor 205 in which pins 238, 240 and 242 are bidirectional I/O pins, an expansion processor 202 having a primary bus address in which a pair of pins 238, 240 and 242 are pulled to logic "1" may also serve as one of sub-buses 220, 226 and 232. In such an embodiment, the pair of pins would be pulled to logic "1" through a corresponding pair of pull-up resistors. The use of such pull-up resistors is well within the understanding of an artisan of ordinary skill, and therefore, have been omitted from FIG. 2 for simplicity.

Each of expansion devices 208, 210, 212, 214, 215, 216, and 218 have a preselected I²C address which represents their I²C address on the device's corresponding sub-bus. After addressing expansion processor 202, the bus master in primary bus 203 sends a data value representing the sub-bus number on which the expansion device resides to expansion processor 202. The bus master then sends the I²C address of the device to expansion processor 202. In an embodiment of the present invention, the sub-bus number and the I²C address of the device on that sub-bus may be represented by a first and second data byte sent to expansion processor 202 during a primary bus 203 device selection/internal pointer write phase.

Expansion processor 202 recognizes the device selection/internal pointer write phase wherein expansion processor 202 then intermediates the transaction between the bus master and the expansion device corresponding to the sub-bus number/address sent in the device selection/internal pointer write phase. Note that the device selection/internal pointer mechanism is not part of the standard PC protocol but is compatible with it. Expansion processor 202 stores the current bus number as the most recently used bus and the address on that bus of the addressed one of expansion devices 208, 210, 212, 214, 215, 216, and 218, as the current address. The addressed one of expansion devices 208, 210, 212, 214, 215, 216, and 218 will be referred to as the target expansion device. The remaining portion of an I²C transfer sequence from the bus master on primary bus 203 is received by expansion processor 202 and echoed to the target expansion device if the transaction between the bus master and the target expansion device is a write to the target expansion device. For a read from the target expansion device, the target expansion device sends its I²C data transfer sequence to expansion processor 202 serving as the bus master for the corresponding sub-bus. Expansion processor 202 then forwards the data to the bus master on primary bus 203 initiating the transaction with the target expansion device, expansion processor 202 then serving as a slave device on primary bus 203.

Expansion processor 202 also intermediates transfer acknowledgment processes. During a write to one of the expansion devices, expansion processor 202 will stretch the clock on primary SCL 206 until an acknowledgment/no acknowledgment (ACK/NACK) response has been received from the target expansion device. Expansion processor 202 then echoes the received response to the bus master on primary bus 203. Note that the clock stretching mechanism is standard in the I²C protocol. If expansion processor 202 receives a NACK response from the target expansion device, the NACK response echoed on primary bus 203 will be detected by the bus master and treated as an error. The bus master will then abort the entire transfer sequence and retry. Expansion processor 202 also verifies the bus number received from the bus master during the device selection/internal address phase. If the value received is not a valid bus number, expansion processor 202 responds with a NACK on primary bus 203.

Expansion processor 202 also responds to protocol errors. This condition is a "hang" on either primary bus 203 or any of sub-bus 220, 226, and 232. For each bit transfer within a byte transfer, expansion processor 202 initializes a timer, and if the bit transfer is not completed in a predetermined time interval, expansion processor 202 will abort both the transfer on primary bus 203 and on the appropriate one of sub-bus 220, 226, and 232. Expansion processor 202 releases primary SDA 204 and primary SCL 206, and will issue a start-data-stop sequence on the appropriate one of the sub-buses to clear the sub-bus. Processor 202 also prepares to receive a start condition. The start condition, stop condition, and start-data-stop sequences are standard states in the I²C protocol and will be described further in conjunction with FIGS. 3A-3B.

The operation of I²C expansion apparatus 200 may be further understood by referring now to FIGS. 3A-3B in which is illustrated a transaction between a bus master on a primary bus and an expansion device on a sub-bus, sub-bus transaction sequence 300, according to the principles of the present invention. Transaction sequence 300 includes primary bus transfer sequence 301 and sub-bus transfer sequence 302.

Sub-bus transaction sequence 300 begins with primary bus transfer sequence 301 initiating a data transfer with start condition 303. When I²C bus is at rest, both SDA 204 and SCL 206 must be "high". Start condition 303 corresponds to a "high" to "low" transition on primary SDA 204 while primary SCL 205 is "high" and is a standard control signal in the I²C protocol. Start 303 is followed by byte 304 constituting seven bits containing the address of expansion processor 202, FIG. 2, on primary bus 203. The last bit of byte 304 is read/write bit 305. Read/write bit 305 may signal a write with a "low" or logic "0" value in accordance with the I²C protocol. Expansion processor 202 responds with ACK 306. Primary bus transfer sequence 301 then continues with the next data bit 307 containing the code for the sub-bus on which the target expansion device resides. Following receipt of byte 307, expansion processor 202 responds with ACK 308. Data byte 309 is then transmitted. Data byte 309 contains the address of the target device on the sub-bus selected in byte 307. Primary bus transfer sequence 301 then enters wait state 310 generated by expansion processor 202 holding primary SCL 206 in a logic "0", or "low", value.

Sub-bus transfer sequence 302 then begins with expansion processor 202 asserting a start bit 311 and then asserting byte 309 on the sub-bus selected in byte 307. Address byte 309 includes read/write bit 312, which signals a write. The target expansion device acknowledges its address with ACK 313. This is echoed by expansion processor 202 to primary bus 203, ACK 314. Sub-bus transfer sequence 302 then enters wait state 315, generated by expansion processor 202 holding the clock and data lines of the sub-bus selected in byte 307.

During wait state 315 of sub-bus transfer sequence 302, primary bus transfer sequence 301 continues with the transmission of data byte 316. Primary bus transfer sequence 301 then enters wait state 317, and expansion processor 202 echoes data byte 316 in sub-bus transfer sequence 302. The target expansion device responds by acknowledging the receipt of data byte 316 with ACK 318 which is then echoed on primary bus 203, ACK 319. Sub-bus transfer sequence 302 then enters wait state 320.

Primary bus transfer sequence 301 then continues with a read operation by issuing start 325 and addressing expansion processor 202, byte 321 which includes read/write bit 322 signaling a read, which may be a "high", or logic "1", value according to the I²C protocol. Primary bus transfer sequence then enters wait state 323. A read operation uses the current target expansion device, wherein a read operation is always preceded by a write to establish the target device. Recall that expansion processor 202 stores the code corresponding to the current expansion bus and the current target device.

Sub-bus transfer sequence 302 continues with expansion processor 202 initiating the read transaction on the sub-bus corresponding to byte 307 with start condition 324 followed by address byte 325. The upper seven bits of address byte 325 correspond to the upper seven bits of address byte 309. The LSB of address byte 325 is read/write bit 326, signaling a read. The target device responds with ACK 327 which is echoed on primary bus 203, ACK 328, by expansion processor 202.

Following ACK 327, the target device sends the first byte of read data byte 329. Expansion processor 202 echoes this in primary bus transfer sequence 301. Following the echo of data byte 329, sub-bus transfer sequence 302 enters wait state 330. The bus master requesting the read from the expansion device acknowledges the first data byte, ACK 331. Primary bus transfer sequence 301 then enters wait

state 332. ACK 331 is echoed by expansion processor 202 onto the expansion bus ACK 333. This informs the target expansion device to send the next data byte 334, which in transaction sequence 300 is a last read data byte. Data byte 334 is echoed in primary bus transfer sequence 301 by expansion processor 202. Because byte 334 is the last data byte to be read, the bus master initiating the read responds with NACK 335, which is echoed on the sub-bus selected by byte 307 by NACK 336. Then, sub-bus transaction sequence 300 ends with stop condition 337 in primary bus transfer sequence 301 which is echoed in sub-bus transaction sequence 302, stop 338. The NACK/STOP sequence is a standard sequence following a last data byte for read transactions within the I²C protocol. Stop conditions 337 and 338 are signaled by a low to high transition in the corresponding serial data line while the associated serial clock line is held "high", or in a logic "1" state.

The operation of expansion processor 202 in a sub-bus transaction sequence, such as sub-bus transaction sequence 300, may be further understood by referring now to FIGS. 4A, 4B, and 4C illustrating a flowchart of I²C bus expansion process 400 according to the present invention. Process 400 initializes on power-up in step 402, and in step 404 snoops primary bus 203 waiting for I²C input addressed to expansion processor 202. On receipt of an address byte signaling the address of expansion processor 202, as previously described in conjunction with FIGS. 3A-3B, process 400 determines if the bus master initiating the transaction is requesting a read or a write, step 406. For a write transaction, expansion processor 202 accepts and stores the sub-bus number on which the target expansion device resides, and in step 410 expansion processor 202 accepts and saves the address of the target device on the sub-bus designated by the sub-bus number from step 408. In step 412, expansion processor 202 sends the device address from step 410 onto the sub-bus from step 408.

In step 414, process 400 determines if an ACK was received from the target expansion device, acknowledging receipt of the address. If an ACK was not received (a NACK was received), then the process proceeds to step 450. In step 450, a determination is made whether an ACK had been previously received from that particular target expansion device. If yes, the process proceeds to step 451 to record a failure for that particular target expansion device. If in step 450, an ACK had not been previously received from that particular target expansion device, then the process proceeds from step 452 to mark as an indication that there is no such particular target expansion device.

The recorded failure in step 451 and/or the indication that the target device does not exist in step 452 may be sent back to the main service processor (e.g., CPU 110) through the primary I²C bus 203. In this way, the service processor can poll each and every device on the I²C bus system to determine where, if any, failures reside. Process 400 then returns to step 404.

If, in step 414, an ACK was received from the target expansion device, the write transaction can proceed. In step 418, process 400 determines if a stop condition is received from the requesting bus master on primary bus 203. If a stop condition was not received, in step 420 a next byte is received from the requesting bus master on primary bus 203, and in step 422 the byte is sent to the target expansion device by expansion processor 202. Process 400 then returns to step 414 to determine if the target expansion device received the byte successfully. Process 400 then continues to receive bytes from the bus master on primary bus 203 and echo them to the target expansion device by looping through steps 418,

420, 422 and 414, until a stop condition is received in step 418. When a stop condition is received, indicating that the write operation is concluded, in step 424, a stop is issued to the sub-bus designated by the sub-bus number received in step 408, and process 400 returns to snoop primary bus 203, in step 404.

If, in step 406, a read operation is signaled, process 400 continues in step 426 by accessing a current sub-bus and expansion device determined in steps 408 and 410, respectively. Thus, a read transaction is always preceded by a write transaction, namely, the device select/internal pointer sequence. In step 428, a byte is read from the target expansion device and, in step 430, transmitted to the primary bus master requesting the transaction.

In step 432, process 400 determines if receipt of the byte transmitted in step 430 is acknowledged. If an ACK is received in step 432, process 400 continues to read bytes by returning to step 428 and looping through steps 428, 430 and 432 until a NACK is received in step 432. Recall, as discussed in conjunction with FIG. 3, that for a read operation, the requesting master signals the last read byte with a NACK in the I²C protocol. Process 400 then continues by issuing a stop to the current sub-bus, in step 424, and returns to step 404 to snoop primary bus 203.

Although the present invention and its advantages have been described in detail, it should be understood that various changes, substitutions and alterations can be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

What is claimed is:

1. a processor;
a primary I²C bus coupled to the processor;
a hub expander coupled to the primary I²C;
an I²C sub-bus coupled to the hub expander;
a bus device coupled to the I²C sub-bus; and
circuitry for determining if the bus device is defective.
2. The system as recited in claim 1, wherein if the defective bus device locks up the I²C sub-bus, the primary I²C bus remains functional.
3. The system as recited in claim 1, wherein the determining circuitry further comprises:
circuitry for addressing and attempting to access the bus device;
circuitry for determining if the bus device responds to the access attempt; and
circuitry for determining that the bus device is defective if the bus device does not respond to the access attempt.
4. The system as recited in claim 3, wherein the circuitry for determining that the bus device is defective if the bus device does not respond to the access attempt further comprises:
circuitry for determining if the bus device had responded to a previous access attempt; and
circuitry for indicating that the bus device is defective if the bus device had responded to the previous access attempt.
5. A method for polling devices for possible errors in an I²C bus system comprising a processor a primary I²C bus coupled to the processor, a hub expander coupled to the primary I²C, an I²C sub-bus coupled to the hub expander, and a bus device coupled to the I²C sub-bus, comprising the step of:
determining if the bus device is defective.
6. The system as recited in claim 5, wherein if the defective bus device locks up the I²C sub-bus, the primary I²C bus remains functional.

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7. The system as recited in claim 5, wherein the determining step further comprises the steps of:

addressing and attempting to access the bus device;

determining if the bus device responds to the access attempt; and

determining that the bus device is defective if the bus device does not respond to the access attempt.

8. The system as recited in claim 7, wherein the step of determining that the bus device is defective if the bus device does not respond to the access attempt further comprises the steps of:

determining if the bus device had responded to a previous access attempt; and

indicating that the bus device is defective if the bus device had responded to the previous access attempt.

9. A bus device comprising:

a hub expander operable for coupling to a primary I²C bus;

one or more modules each including a storage device storing information about its particular module;

one or more I²C sub-busses, each coupling one of the modules to the hub expander; and

circuitry for determining if one of the one or more modules is defective.

10. The bus device as recited in claim 9, wherein if the defective module locks up its respective I²C sub-bus, the primary I²C bus remains functional.

11. The bus device as recited in claim 9, wherein the determining circuitry further comprises:

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circuitry for addressing and attempting to access the one of the one or more modules;

circuitry for determining if the one of the one or more modules responds to the access attempt; and

circuitry for determining that the one of the one or more modules is defective if the one of the one or more modules does not respond to the access attempt.

12. The bus device as recited in claim 11, wherein the circuitry for determining that the one of the one or more modules is defective if the one of the one or more modules does not respond to the access attempt further comprises:

circuitry for determining if the one of the one or more modules had responded to a previous access attempt; and

circuitry for indicating that the one of the one or more modules is defective if the one of the one or more modules had responded to the previous access attempt.

13. The bus device as recited in claim 9, wherein the bus device is a memory device, and wherein the one or more modules are memory modules.

14. The bus device as recited in claim 13, wherein the memory modules are DIMMs.

15. The bus device as recited in claim 11, wherein the bus device is a memory device, and wherein the one or more modules are memory modules.

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